CLAIMS

What is claimed is:

1. A method comprising:

(a) driving a plurality of data symbols into a transmission line while simultaneously driving the plurality of data symbols into another node;

(b) determining a difference between a signal level from the transmission line and a signal level from the other node while performing (a), and applying the difference to a signal input of a comparator, the comparator having a substantially variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between a signal level at the comparator input and the variable reference level; and

(c) applying one of a plurality of binary values to an offset control input of the comparator, to adjust the variable reference level prior to the comparator performing the comparison.

2. The method of claim 1 further comprising:

sampling a signal from the transmission line and a signal from the other node while performing (a), prior to determining the difference.

3. The method of claim 1 further comprising:

updating the binary value that is applied to the offset control input of the comparator as a function of the data symbol being driven.

4. The method of claim 1 further comprising:

clocking the comparator at the same frequency as sampling the signal from the transmission line, updating the binary value, and driving the plurality of data symbols.

5. A circuit comprising:

a first driver having an output to be coupled to a transmission line;

a second driver being a replica of the first driver, the first and second drivers having inputs being coupled to receive the same sequence of outgoing data symbols;

a subtraction circuit having a first input to be coupled to the transmission line and a second input coupled to the output of the second driver;

a comparator having an input coupled to an output of the subtraction circuit, the comparator having a substantially variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between a signal level at the comparator input and the variable reference level; and

a control circuit having an output that is coupled to an offset control input of the comparator and is to provide a first binary value that corrects for one of a mismatch between the first and second drivers and a mismatch in the subtraction circuit.

6. The circuit of claim 5 wherein the control circuit further comprises a multiplexer having an output being coupled to the offset control input and a first input coupled to receive the first binary value, and a timing circuit coupled to control the multiplexer so that the variable reference level of the comparator is adjusted, according to the first binary value, prior to a transitioning of the transmission line signal between different data symbol levels.

7. The circuit of claim 6 wherein the multiplexer further includes a second input coupled to receive a second binary value which represents the variable reference level being approximately at the midpoint between two adjacent, nominal data symbol levels defined for the transmission line signal.

8. The circuit of claim 7 wherein the first binary value represents a difference between the transmission line signal and the second driver output signal during the transitioning of the transmission line signal between the different data symbol levels.

9. The circuit of claim 8 wherein the comparator input is differential.

10. The circuit of claim 9 wherein the comparator has a differential input provided by first and second differential pairs each being intentionally unbalanced, each pair having first and second output nodes, the first output

node of the first pair being coupled to the second output node of the second pair, the second output node of the first pair being coupled to the first output node of the second pair, and first and second variable current generators coupled to control respective tail currents of the first and second differential pairs.

11. The circuit of claim 9 wherein the subtraction circuit further includes a sampler circuit coupled to sample signals at the first and second inputs.

12. A system comprising:

a printed wiring board on which a parallel bus is formed, an integrated circuit (IC) chip package being operatively installed on the board to communicate using the parallel bus, the package having an IC chip that includes a logic function section and an I/O section as an interface between the logic function section and the bus, the I/O section having a bus receiver in which a first near end driver whose output is coupled to the bus, a second near end driver being a replica of the first driver, the first and second drivers having inputs being coupled to receive the same sequence of outgoing data symbols, a subtraction circuit having a first input coupled to the transmission line and a second input coupled to the output of the second driver, a comparator having an input coupled to an output of the subtraction circuit, the comparator having a substantially variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between a signal level at the comparator input and the variable reference level, and a control circuit having an output that is coupled to an offset control input of the comparator and is to provide a binary value that represents an output signal level of the subtraction circuit.

13. The system of claim 12 wherein the logic function section is a microprocessor.

14. The system of claim 12 wherein the logic function section is a memory controller.

15. The system of claim 12 wherein the logic function section is a bus bridge.

16. The system of claim 12 wherein the binary value represents a first adjustment to the variable reference level of the comparator, and the control circuit further includes a timing circuit coupled so that the variable reference level of the comparator is adjusted, according to the binary value, prior to a transitioning of the transmission line signal between different data symbol levels.

17. A circuit comprising:

means for transmitting a plurality of near end data symbols while allowing the simultaneous receipt of a plurality of far end data symbols;

means for emulating the transmission of the plurality of near end data symbols without allowing receipt of the plurality of far end data symbols;

means for generating a difference between a signal level that represents one of the plurality of transmitted near end data symbols and a signal level that represents an emulation of said one of the plurality of transmitted near end data symbols;

means for comparing the difference to an implied reference level without requiring a separate voltage input to receive the implied reference level; and

means for adjusting the implied reference level to correct for one of a mismatch between the transmission and emulation means and a mismatch in the difference generation means.

18. The circuit of claim 17 further comprising:

means for timing the adjustment of the implied reference level, so that the adjustment occurs prior to the occurrence of a signal level change at an input of the comparison means, wherein the signal level change represents the transmission of one of the plurality of near end data symbol levels.

19. The circuit of claim 18 further comprising:

means for setting the implied reference level to represent approximately the midpoint between two adjacent, nominal data symbol levels defined for a transmission line signal.

20. The circuit of claim 19 wherein the adjustment means is to adjust the implied reference level by an amount approximately equal to the difference between the signal level that represents one of the plurality of transmitted near end data symbols and the signal level that represents the emulation of said one of the plurality of transmitted near end data symbols.

21. The circuit of claim 17 further comprising:

means for capturing and holding the signal level that represents one of the plurality of transmitted near end data symbols and the signal level that represents an emulation of said one of the plurality of transmitted near end data symbols.